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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/825,365	04/16/2004	Chang Ycon Kim	8733.1032.00-US	8096

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WASHINGTON, DC 20006

EXAMINER
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TSEGAYE, DANIEL

ART UNIT	PAPER NUMBER
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2629

MAIL DATE	DELIVERY MODE
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09/21/2007

PAPER

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

## Office Action Summary

Application No.

10/825,365

Applicant(s)

KIM ET AL.

Examiner

DANIEL TSEGAYE

Art Unit

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

### Status

- 1) ☒ Responsive to communication(s) filed on 28 June 2007.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

### Disposition of Claims

- 4) ☒ Claim(s) 1-22 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-22 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

### Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some \* c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

### Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO/SB/08)  
Paper No(s)/Mail Date 06/28/2007.
- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_\_.
- 5) ☐ Notice of Informal Patent Application
- 6) ☐ Other: \_\_\_\_\_.

**DETAILED ACTION**

***Response to Amendment***

1. The amendment filed on 06/28/2007 has been entered and considered by the examiner.

***Priority***

2. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

***Claim Rejections - 35 USC § 103***

3. The following is a quotation of 35 U.S.C. 103(e) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. Claims 1,2,8,9-12,13,15,17-19 are rejected under 35 U.S.C. 103(e) as being unpatentable over Ishizuka (U.S. Pat # 6,965,362) in view of Tsuge (U.S Pub #2005/030264).

As to claim 17, Ishizuka disclose an electro-luminescence display device, comprising:

gate lines (cathode lines, e.g., B<sub>1</sub>-B<sub>2</sub>);

data lines (anode lines, e.g., A<sub>1</sub>-A<sub>m</sub>) crossing the gate lines (see col.5, lines 64-65);

pixel cells at crossings of the gate lines and the data lines (see col. 5, lines 58-62);

a gate driver (13) that sequentially applies a gate signal to the gate lines (cathode lines) during one horizontal period (see col.6, lines 4-15); and

a plurality of data driving circuits (e.g., 17<sub>1</sub>-17<sub>m</sub> and corresponding  $v_p$ , see Fig. 7) having a voltage driver ( $v_p$ ) that applies voltage signal to the data lines (anode line e.g., A<sub>1</sub>-A<sub>m</sub>) corresponding to image data and a current driver (e.g., 17<sub>1</sub>-17<sub>m</sub>) that allows the current signals corresponding to the image data to flow from the pixel cells (see col.6, lines 33-39 and also see from col.6, lines 61-67 to col.7, lines 1-8). Ishizuka do not teaches that applies voltage signals and a current signal within the horizontal period. Tsuge teaches applying voltage signals to the data lines corresponding to image data with in horizontal period and a current driver that allows the current signals corresponding to the image data to flow from the pixel cells within the horizontal period (see [0020], [0022] , [0023] and claim 2).

Therefore, it would have been obvious to one of ordinary skill in the art at time the invention was made to applying voltage signals to the data lines corresponding to image data within horizontal period and a current driver that allows the current signals corresponding to the image data to flow from the pixel cells within the horizontal period to light emitting panel of Ishizuka so as to prevent the occurrence of flickering (see [0033] of Tsuge).

As to claims 1 and 18, these claims differs from claim 17 only in the limitation “apply voltage signals to the pixel cells during a first time of the horizontal period and

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applying current signals to the pixel cells during a second time after the first time of the horizontal period" additionally recited. Tsuge clearly teaches apply voltage signals to the pixel cells during a first time of the horizontal period (e.g. precharge with voltage first) and applying current signals to the pixel cells during a second time after the first time of the horizontal period (e.g. precharge the voltage first and switch to signal current source second, see [0020]).

As to claim 9, Ishizuka teaches an electro-luminescence display device, comprising:

applying a gate signal to pixel cells along a specific horizontal line (e.g.,  $B_1$ ) during a horizontal period (see col.6, 9-15);

applying a voltage value ( $v_p$ ) corresponding to image data to the pixel cells during a first time ( $T_1$ ).

applying a current value (e.g.,  $17_1$ ) corresponding to the image data to the pixel cells (e.g.,  $E_{1,1}$ ) during a second time after the first time to display an image corresponding to the image data ( see col.6, lines 24-39). Ishizuka '362 does not teach pre-charge the pixel cells and within the horizontal period. Tsuge teaches applying a voltage value corresponding to image data to the pixel cells during the first time to pre-charge the pixel cells as recited in the claim (see [0022], [0027]). Thus combining Ishizuka and Tsuge would meet the claimed limitation for the same reasons as mentioned in claim1.

As to claim 10, Ishizuka teaches wherein applying a voltage value and applying a current value are repeated every horizontal period (see col.7, lines 9-18).

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As to claim 11, Ishizuka '362 teaches wherein the first time (e.g. referring to Fig. 4,  $T_1=t$ ) is less than the second time (e.g. referring to Fig. 4,  $T_2=2t$ ).

As to claims 8, 12 and 16, Tsuge teaches wherein applying a voltage value includes charging a storage capacitor (see [0139], [0181] and [0280]).

As to claim 13, this claim differs from claim 1 only in that claim 1 is apparatus whereas claim 13 is method. In addition, claim 13 recite the limitation "applying a gate signal from a gate driver during each horizontal period to select pixel cells along specific horizontal line". Ishizuka clearly teaches that applying a gate signal from a gate driver (13) during each horizontal period to select pixel cells (e.g.,  $E_{1,1}$  Fig.7) along specific horizontal line (e.g.,  $B_1$ , and also, see col.6, 9-15).

As to claims 2, 15 and 19, note the discussion above, Ishizuka teaches wherein the first time ( $T_1$ ) is shorter than the second time ( $T_2$ ).

5. Claims 3, 5-7, 21-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ishizuka (U.S Pat # 6,965,362) in view of Tsuge, further in view Ishizuka et al. (U.S Pat # 6,756,951)

As to claims 3 and 21, note the discussion of Ishizuka '362 and Tsuge above. Ishizuka '362 teaches, a voltage driver ( $v_p$ , see Fig.7) that applies voltage signals to the data lines (e.g.,  $A_1-A_m$ ) corresponding to image data (4) (see Fig. 4); and a current driver (e.g., 17<sub>1</sub>, see Fig.7) that allows the current signals corresponding to the image data (4) to flow from the pixel cells (see from col.6, lines 61-67 to col.7, lines 1-8). Ishizuka '362 does not teaches wherein each of the plurality of data driving circuit.

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Ishizuka '951 teaches wherein each of the plurality of data driving circuits (e.g., 201,202 and 203).

Therefore, it would have been obvious to one of ordinary skill in the art at time the invention was made to have used each of the plurality of data driving circuits of Ishizuka '951 to light emitting panel of Ishizuka '362 because more data driving circuit make the display panel uniform (see col.3, lines 1-4 of Ishizuka '951).

As to claim 5, Ishizuka '362 teaches wherein the voltage driver includes;

a plurality of first switches (e.g., 16<sub>1</sub>&16<sub>m</sub>) in the voltage driving block (14) and each of the data lines, wherein the first switches are turned on by a control signal (see col.6, lines 24-31 of Ishizuka '362). Ishizuka '952 teaches number of driving blocks (201-202). Thus combining Ishizuka '362 and Ishizuka '952 would meet the claim limitations.

As to claims 6 and 22, Ishizuka '951 teaches wherein said current driver includes;

a plurality of current driving blocks (e.g., 201,202 and 203) corresponding to each data line that drive the current signal in response to the image data, said current driving blocks having i blocks (e.g., 201,202 and 203); and

a plurality of second switches (s<sub>1</sub>-s<sub>m</sub>) between each of the current driving blocks (e.g., 202 'Ishizuka ') and each of the data lines (e.g., A<sub>1</sub>) and wherein the second switches (s<sub>1</sub>-s<sub>m</sub>) are turned on by a control signal (see from col.6, lines 54-67 to col.7, lines1-10).

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As to claim 7, Ishizuka '362 teaches wherein the control signal remains at a first level (e.g., toward  $v_p$ ) during the first time (e.g., during  $T_1=t$ ) and remaining at second level (e.g., toward current source) during the second time (e.g., during  $T_2=2t$ )(see col.6, lines 24-31).

6. Claims 4,14 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ishizuka (U.S. Pat # 6,965,362) in view of Tsuge, and further in view of Ha et al. (U.S Pat #7,030,842).

As to claims 4 and 20, Ha teaches a gamma voltage driver (46) that applies a plurality of gamma voltage levels to the voltage driver (44) so as to generate the voltage signal (see col.8, lines 25-33).

Therefore, it would have been obvious to one of ordinary skill in the art at time the invention was made to have provided a gamma voltage driver that applies a plurality of gamma voltage levels to the voltage driver so as to generate the voltage signal as taught by Ha to light emitting panel of Ishizuka '362 modified by Tsuge because the gamma voltages generators applying different gamma voltages would provide the pictures are displayable by the panels at a substantially uniform brightness (see col.7, lines 1-3)

As to claim 14, Ha teaches applying the voltage value to the pixel cells (48) includes selecting one of a plurality of gamma voltage (e.g., Gamma one, see col.3, lines 48-50) values according to the image data to apply to the pixel cells (see col.8 lines 35-38).



### ***Response to Arguments***

7. Applicant's arguments with respect to claim 1, 9, 13 and 17 have been considered but are moot in view of the new ground(s) of rejection.

In view of amendment, the reference of Tsuge has been added for new ground of rejections.

### **Conclusion**

8. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the mailing date of this final action.

### **Inquiries**


9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to DANIEL TSEGAYE whose telephone number is 571 270-1715. The examiner can normally be reached on Monday-Friday, 8:00-5:00 EST.

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If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, CHANH NGUYEN can be reached on 571 272 7772. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

D Tsegaye  
9/10/2007

  
CHANH D. NGUYEN  
SUPERVISORY PATENT EXAMINER